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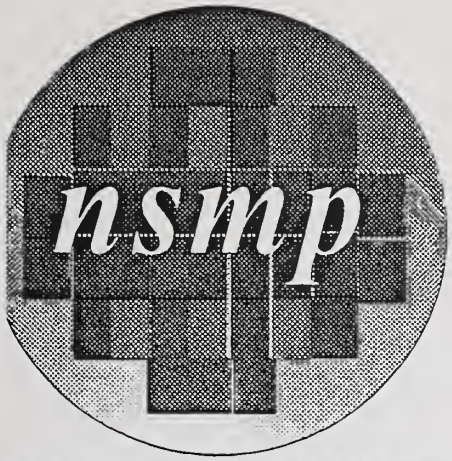

National Semiconductor Metrology Program

Project Portfolio FY 1996

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Edited by

David S. Yaney
and Alice D. Settle-Raskin
Office of Microelectronics Programs

U.S. DEPARTMENT OF COMMERCE

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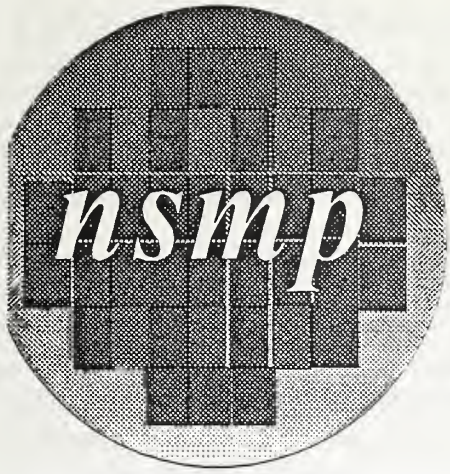

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David S. Yaney and
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Office of Microelectronics Programs

U.S. DEPARTMENT OF COMMERCE
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Technology Administration
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June 1996

Foreword

The National Semiconductor Metrology Program (NSMP) is a NIST-wide effort designed to meet the highest priority measurement needs of the semiconductor industry as expressed by the *National Technology Roadmap for Semiconductors* and other authoritative industry sources. The NSMP was established in 1994 with a strong focus on mainstream silicon CMOS technology and an ultimate funding goal of $25 million annually. Current annual funding of approximately $11 million supports the 23 internal projects which are summarized in this Project Portfolio booklet.

The NSMP is operated by NIST's Office of Microelectronics Programs, which also manages NIST's relationships with the Semiconductor Industry Association (SIA), SEMATECH, and the Semiconductor Research Corporation (SRC). These include NIST's memberships on the SIA committees that develop the *Roadmap* and numerous SRC technical management committees. In addition, NIST is active in the semiconductor standards development activities of ASTM, Deutsches Institut für Normung, Electronic Industries Association, International Organization for Standardization, and Semiconductor Equipment and Materials International.

For further information about our program or how we can serve you, please contact us as follows:

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Please note:

Certain commercial equipment and/or software is identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purposes.

References made to the National Technology Roadmap for Semiconductors (NTRS) apply to the most recent edition dated 1994. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

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Dimensional Metrology at the Nanometer Level

The scanning electron microscope (SEM) has become the familiar instrument of choice for in-line process inspection and metrology. Scanning probe instruments have recently emerged to both complement and extend the capabilities of the SEM. The atomic force microscope (AFM) is the most significant of these new instruments for semiconductor applications since it is capable of nanometer resolution on features of virtually any material and can operate directly in the clean room environment. NIST has a 3-element program spanning two groups to extend the technical understanding of these instruments and expedite their application in the industry.

First, NIST has constructed a calibrated metrology AFM (C-AFM) with 3-axis interferometric determination of tip position. This is a research instrument specifically designed to aid development of suitable AFM standards, and is capable of nanometer-scale dimensional measurements, with metrology traceable to the wavelength of light in all three axes. Its pitch, height, and width measurement capabilities have been evaluated and are presently at or near desired performance levels. Pitches ranging up to 20 μm can be measured with uncertainties of ~0.1 %, and heights ranging up to 1 μm can be measured with uncertainties of ~2%. The widths of sub-micron near-vertical features can be measured to ~30 nm, with uncertainty due mostly to correcting for the size of the tip. In related collaborative work with the University of Maryland, a series of silicon samples with single atom steps have been fabricated and imaged in the C-AFM. These samples have considerable potential as fundamental step height and possibly roughness standards.

The second thrust of the NIST work is to demonstrate capability for calibrated linewidth and sidewall angle measurements on a commercial noncontact scanning probe instrument. This work is managed through a Cooperative Research and Development Agreement (CRADA) with an IC manufacturer and utilizes an instrument installed in their fabrication facility. Evaluation of both commercially available and prototype tip characterization and linewidth artifacts are the major component of this work. A reversal technique for the measurement of sidewall angle and tip size correction for the measurement of linewidth are major features of the approach taken in this work. In a first phase comparison between these AFM measurements and cross sectional TEM, good agreement was found with about 30 nm uncertainty in linewidth and a one degree uncertainty in sidewall angle. For the next phase of this effort, several samples will be used and the consistency of several instruments (different AFMs and TEM) with respect to the sample set will be examined. The goal of this study will be to further quantify measurement uncertainties and develop suitable standards for characterization of both conical and "boot" shaped tips.

Finally, NIST is creating yet another unique tool through the marriage of a compact commercial scanned probe instrument with a high-resolution field emission SEM. This work is being facilitated through a CRADA with a commercial scanned probe instrument company. The combination of these two techniques is expected to yield an instrument with superior qualitative and quantitative capabilities - a "measurement engine" for advanced microelectronics. At this time, the new integrated tool has just been installed and is undergoing optimization.

[Metrology is mentioned throughout the Lithography chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS). Requirements are defined on page 85, Tables 17 and 18. Potential solutions are on pages 89 and 90; Tables 15 and 16. Metrology is cited as a high-priority need on page 91.]

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Plasma and CVD Process Measurements

Improved characterization and control of etching and deposition plasmas are required for the next generation of semiconductor fab processes. NIST is addressing the metrology-related aspects of this problem through development of diagnostic tools and techniques on a simple yet highly-relevant reference platform. These tools are applied to probe the microscopic characteristics of the discharge such as species density, electron and ion energies, and optical emission characteristics. While these parameters are the most appropriate to describe plasma conditions, macroscopic parameters (power, pressure, and gas flow) are used as control parameters today because the complex relationships among the microscopic variables are uncharacterized. A major task is development of characterization methods to translate microscopic plasma parameters into macroscopic control parameters.

Much of this work uses a universal plasma reactor called the GEC rf Reference Cell (GEC from the Gaseous Electronics Conference where the idea was conceived). More than 25 such cells are currently in use as a standard, reproducible platform for accurate intercomparisons of experimental data and results from plasma models. The GEC cells at NIST are equipped with a wide range of diagnostics including RF current and waveform analysis, Langmuir probes, optical emission, mass spectrometry with ion energy analysis, laser-induced fluorescence (LIF), and spectroscopic ellipsometry.

To date, these diagnostics have been applied to plasmas of Ar, He, O_2, H_2, N_2, SF_6, CF_4, Cl_2 and various mixtures of these gases. Results have identified diagnostics applicable to industrial reactors and the limits of those techniques, as well as the generation of basic plasma data suitable for the validation of various discharge models. Examples of specific results include:

1. A complete electrical characterization of the GEC cell resulting in improved plasma reproducibility. This knowledge has already been successfully applied to industrial reactors, and has recently been extended to processing gases, such as SF_6 and NF_3.
2. Development of a uniformity and reproducibility monitor for industrial reactors utilizing optical emission measurements.
3. Determination of neutral and ionic species in SF_6-containing plasmas, including measurement of the degree of gas dissociation for different plasma conditions.
4. Measurement of metastable and radical densities in CF_4-containing discharges for validation of plasma models.

Several related projects supply basic support for modeling electric discharges used in semiconductor fabrication. These include modeling of particle formation in plasma-enhanced and thermal CVD reactors, measurement and analysis of fundamental reference data for industrially-relevant gases, and dissemination of experimental results to more than 20 different laboratories.

Future plans include:

1. Development of a new reference reactor more closely resembling industrial designs.
2. Extension of all diagnostic techniques for application to inductively-coupled discharges.
3. Development of measurement techniques for frequency-compensated electric probes.
4. Continuing measurement, assessment, and distribution (via Internet) of fundamental data necessary to model and improve commercial reactors.
5. Investigate radical formation mechanisms in CH_xF_y plasmas using 2-D LIF.

[The degree of empiricism embodied in the plasma tools of today is so well-known that it almost escapes mention in the NTRS. Needs for modeling (for process control) are indicated in Figure 31, page 129. Modeling and simulation of etch and deposition processes are essential for interconnect - see page 105 and Table 25. PECVD is one of the upper dielectric layer deposition tools mentioned in Figure 23 as a potential solution for interconnect.]

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Optical CD and Overlay Metrology

Tighter tolerances on CD measurements in wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these measurements.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch artifacts in the range of 0.5μm to 30 μm are currently certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm.[1] These standards are being compared with linewidth measurements in other national standards laboratories, with excellent results to date.[2]

An ultraviolet transmission microscope with quartz optics has been constructed that will replace the existing green light system mentioned above. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. It is also able to accept larger sample sizes.

Synchronous data acquisition techniques and subsequent data analysis with well-developed edge detection algorithms along with reduced transmission of UV through the chrome and reduced instrument vibration will offer substantially improved linewidth uncertainties.

Recent publications from NIST have outlined a new technique for measurement of photomask linewidths called Emulated Stepper Aerial Image Measurement which is expected to reduce uncertainties by 50% or more.[3] The ultraviolet microscope is being enhanced with the capabilities necessary to assess and verify this promising new concept.

The overlay metrology program is investigating and designing a new set of overlay standards. These artifacts will consist of a tool box set that will allow users to align their particular overlay instrument properly and thereby eliminate tool-induced-shift. The use of alignment standards will be followed by calibration with a conventional box-in-box overlay pattern. NIST is also developing a magnification standard for optical microscopes (SRM 2800) with certified pitch patterns from 1 cm to 1 μm to be produced on standard size slides.

To meet future challenges in overlay metrology, design and construction is underway for a state-of-the-art reflection mode confocal microscope at NIST. This instrument will also utilize a Stewart platform. Three-axis interferometry will monitor sample position and a collimated laser beam coupled with a quadrant detector will monitor stage tilt. Resolution is expected to be better than 0.2 μm. A CCD camera and image acquisition electronics will enable general use of the instrument in reflection mode on semiconductor (and other non-transparent) samples.

[NTRS references are identical to those given for the Dimension Metrology work on page 1.]

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[1] J. Potzick, "Re-evaluation of the Accuracy of NIST Photomask Linewidth Standards," Proceedings of the SPIE Symposium on Microlithography, Vol. 2439-20, Santa Clara, Calif. (1995)

[2] Jim Potzick, John Nunn (NPL), "International Comparison of Photomask Linewidth Standards: NPL-NIST," Proceedings of the SPIE Symposium on Microlithography, Vol. 2725-08, Santa Clara, Calif. (1996).

[3] J. Potzick, "Improved Photomask Metrology through Exposure Emulation," Proceedings of Photomask Japan '95: Symposium on Photomask and X-ray MaskTechnology II, SPIE, vol. 2512-61, Bellingham, Wash., pp 274-280 (April 1995).

Fundamental Process Control Metrology for Gases

Gas pressure, composition, and flow are fundamental operating variables in many semiconductor fab processes. NIST efforts in this important area have a dual focus - first, to ensure that the technical underpinnings of the measurements (including standards and calibration procedures) are available and widely disseminated. Second, NIST is examining the performance characteristics of process monitoring and control equipment to permit their optimum use by the industry.

NIST maintains state-of-the-art vacuum (pressure) standards and calibration services for inert gases and makes these available to a broad spectrum of users. However, standards for reactive gases important to the semiconductor industry are almost nonexistent. NIST is addressing this need with work emphasizing measurement of the partial pressures of low-level contaminants in the process chamber with an initial focus on water.

Real-time monitoring of contaminants and gas composition in a process chamber also requires reliable process monitoring equipment. Preliminary NIST studies of commercial residual gas analyzers (RGAs)[1] found undesirable performance characteristics in several instruments. These experimental studies have been extended to include additional RGAs, including one of the new "small-geometry" quadrupoles and a magnetic sector instrument, and have been complemented by theoretical modeling which has provided guidance for optimized instrument performance at the higher pressures often encountered in semiconductor processing. The latest experimental results have been obtained with a NIST automated calibration system that was designed to be adapted for the in-situ calibration of RGAs mounted on process chambers.

Responding to the SEMI/SEMATECH Thermal Mass Flow Meter Working Group, NIST is extending the range and improving the uncertainty of gas flow standards. An initial effort has resulted in a new standard for flows of inert gases between 0.1 sccm and 1000 sccm with corresponding uncertainties from 0.1% to 0.05%. A second standard under construction will extend the range to 10 slm and be compatible with some reactive gases. A prototype laminar flowmeter transfer standard, covering the range 0.1 sccm to 1000 sccm, has demonstrated a repeatability of 0.1% or better. This unit can be adapted to check flow standards in the field.

NIST flow standards are being used in performance studies of the commercial thermal-mass flow controllers commonly used for flow control in semiconductor process equipment. Initial results,[2] for low-range (2sccm to 5 sccm) units from five different manufacturers, show significant errors in some instruments but better performance than specified in others.

[Residual gas analysis is mentioned in the NTRS on page 125. Fluid purity and residual matter in vacuo are discussed on page 127 and in Table 34. Key impurity levels in gases range down to a volume fraction of 10^{-11} (10 ppt) by the year 2007. Figure 30 outlines potential solutions.]

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[1]C. R. Tilford, *Semiconductor Characterization: Present Status and Future Needs,* W.M. Bullis, D.G. Seiler and A.C. Diebold, Eds., (AIP, New York, 1996), pp. 252-255

[2]S. A. Tison, to be published in *J. Vac. Sci. Technol. A 14, No. 4 (1996)*

Materials and Bulk Processes Measurements

Ellipsometry and Thin Films: Measurements are now in progress at NIST and a metrology company on a set of artifacts which should provide information needed to establish the level of uncertainty for those measurements between the two labs. Preliminary results should be available by September1996 with a more complete determination completed by March 1997. Concurrent is an effort to develop a program to provide for a NIST Traceable Reference Material (NTRM) for thin films used in the semiconductor industry. The program would involve multiple collaborative efforts with laboratories providing traceable standards to industry. The experimental design and procedural outline will be completed by October 1996. Calculated thickness of the films refractive indices, as well as measured values of the ellipsometric parameters Δ and Ψ for the single wavelength of λ=633 nm and at both the principal angle of incidence and angle of incidence equal 70°, will be evaluated during the study. An evaluation of the viability of this effort will be made by October 1997.

In order to improve the utility of in-situ optical monitoring of silicon thin-film fabrication process, NIST is embarking on a program of developing accurate optical-constant data for silicon films at processing temperature. A custom-built UHV chamber with spectroscopic ellipsometer, RGA, and other instruments, and capable of 1000°C will be installed at NIST during the summer of 1996. Published data for silicon substrates, SiO_2 and other films, should begin by mid 1997.

Doping Profiles: The detailed 2D and 3D shape and position of submicrometer doping profiles is fundamentally responsible for much of the performance and hot-carrier reliability of modern devices. Today this information is largely inferred through relative comparisons between the output from process simulators and a sequence of device experiments (on a case-by-case basis) since the detailed data needed to calibrate the simulators have not been available NIST has constructed both a new instrument and the required software analysis tools to change this situation The scanning capacitance microscope (SCM) is based on the more-familiar atomic force microscope (AFM), but instead images the differential capacitance between a conducting probe and a wafer as a function of x-y position and dc bias. Coupled with the rigorous 2D and 3D numerical solution of Poisson's equation in a workstation environment, NIST has measured 2Dand 3D doping profiles with better than 30 nm spatial resolution Current work is extending the technique to properly incorporate the topography associated with front-end IC processes.

A feedback circuit has been constructed to maintain the differential capacitance constant as the probe moves over the surface; the voltage swing needed to accomplish this becomes the measured signal. This method improves the resolution and signal linearity. A quasi-2D model based on 1D equations for MOS structures has been developed to obtain very fast conversion from measured data to doping profiles. Comparisons with the full 2D and 3D models have shown the strengths and limitations of this approximate method. A series of structures with doping profiles determined by other methods will be measured by the SCM and modeled to extract doping densities. This compilation of carefully measured and modeled data will be completed by October 1997.

[Thin film properties and doping distributions are discussed throughout the Materials and Bulk Processes and Interconnect chapters of the NTRS (pages 94, 106, 110, 119, 122, and 128; Figures 17, 25 and 31; Tables 25, 30, 32, 33, and 35). In-situ metrology of process performance will require optical measurements in high temperature environments, but these properties are largely unknown.]

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Moisture Concentration Measurements in Process Gases

Moisture is a pervasive contaminant in semiconductor process gases. Current water-vapor concentration-measurement standards are limited to levels above a volume fraction of 2×10^{-6} ($2\ ppm_v$)while fab processes for submicron devices require measurements of humidity levels in the ppb range. Improved measurement standards are needed to provide a sound basis for evaluation of existing measurement technology and development of improved methods useful for both diagnostic and on-line measurement. Both absolute and working standards are needed to support reliable measurements at these low levels. Working standards take the form of precision humidity generators that saturate input gas streams with known moisture concentrations. Absolute moisture concentration measurements are made using gravimetric methods, i.e., a gravimetric hygrometer, that separates and quantifies both the moisture and carrier gas. NIST is developing both capabilities.

NIST has recently fabricated a primary standard hygrometer with a lower operating point anticipated to lie between a volume fraction of 10^{-5} ($10\ ppm_v$) and a volume fraction of 10^{-4} ($100\ ppm_v$). It will be used to characterize precision humidity generators that function as working standards and have operating ranges extending into the ppb region. Once a generator's operation is demonstrated over the range afforded by the gravimetric hygrometer, it can be used over its full operating range. A new precision generator, the low-frost-point moisture generator (LFPG), is nearing completion. Its operating range is approximately a volume fraction of 10^{-8} ($10\ ppb_v$) to a volume fraction of 5×10^{-4} ($500\ ppm_v$). It will be the working standard NIST uses to generate known moisture concentration gases at these levels, is directly related to fundamental measurement standards and is fabricated to conform with high-purity gas-handling technology common to IC manufacturing.

Measurement methods capable of detecting moisture at levels in the volume fraction of 10^{-9} ($1\ ppb_v$) to the volume fraction of 10^{-5}($10{,}000\ ppb_v$) range were surveyed. Optical spectroscopic techniques are being pursued because they have robust measurement capabilities and good sensitivities at these low concentrations. An absorption technique using a "ring-down cavity" method has effective absorption pathlengths of several kilometers for a 1 m cell length. This approach has been demonstrated to have the capability to make absolute species concentration measurements. This recently completed demonstration used pulsed laser sources. Diode laser sources operating in the near IR will be used to provide reliable, narrow band cavity excitation for water vapor. (This technique also has the potential for on-line measurement capability for process monitoring.) Spectroscopic water absorption features near a wavelength of 1.39 μm will be used. Determination of the fundamental line strengths in this spectroscopic region will use both gravimetric methods directly and the LFPG to measure these over several orders of magnitude. Once determined, these fundamental physical constants function as primary measurement standards and provide the means to extend optical techniques over many orders of magnitude with the potential to make reliable measurements into the ppt region.

[The NTRS discusses moisture in gases on page 125; Figure 30; and Table 34. There is a clear call to relate purity of fluids to the performance of processes and devices, thereby avoiding unnecessary materials costs (pages 127 and 131).]

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Metrology for Contamination-Free Manufacturing

NIST is addressing issues associated with the chemistry of particle formation in thermal and plasma reactors and with the development of micro-contamination standards. Improving the current limited understanding of chemical mechanisms causing the generation and growth of particles in the gas phase is critical to minimizing spontaneous particle formation in process reactors. Efforts here will address the measurement and modeling of particle growth phenomena as a basis for extension of particle metrology. The 1996 project plan includes: (1) commissioning a rotating disk CVD reactor; (2) applying numerical models of flow and temperature fields with particle injection and tracking capability; (3) using the models for investigation of model-based controller characteristics; and (4) developing a facility for particle sizing and calibration. The particle size range being considered is 0.07 μm to 0.30 μm.

Combined experimental and modeling efforts focus on a spinning-disk reactor incorporating flow, chemistry and aerosol formation and transport control. A model of the reactor has been developed that is a modification of the Sandia National Laboratories SPIN code and will be used to develop a model of particle formation during deposition. The principal goal of the work is to assess the effects of changes in reactor operating conditions on the levels of wafer contamination, some of which is attributable to particle transport to the wafer surface. The model will be tested against data obtained from the reactor with a variety of optical measurement methods.

Additional modeling efforts focused on studies of wafer contamination during processing in barrel-type CVD reactors. This involved development of a mode for the transport of micron-sized particles which indicated that such reactor may be susceptible to the formation of particle attractors near the wafer surface. These attractors entrain particles of a certain size distribution and hold them stationary in the flow. A novel treatment of the flow had involved the use of dynamical system theory to analyze particle behavior in this vicinity.

In a related effort, NIST completed a short-term project with SEMATECH and member companies to determine detection thresholds and analysis of common particles. The goal of the effort was to find the minimum particle size detectable with two widely-used surface analytical techniques - time-of-flight secondary-ion mass spectrometry (TOF-SIMS) and auger electron spectroscopy. NIST prepared, classified, and deposited particles of both aluminum and aluminum oxide on 25 mm silicon wafers at densities of about 3000 particles/mm^2. Particle sizes were nominally 0.1 μm, 0.3 μm and 0.5 μm. General results were that the 0.3 μm and 0.5 μm particles were detectable for both methods and compositions. Efforts continue to form and characterize small particles to develop measurement methods and techniques for particle standards consistent with needs of the semiconductor industry.

[Particle contamination is one important class of CFM topics in the NTRS. Metrology for 0.1 μm particles and smaller is essential for lithography at 0.25 μm and beyond (Table 17), interconnect (Tables 21 and 26; pages 104 and 105), materials and bulk processes (pages 10, 112, 115, 119, 122, 125 and 128; Figures 25, 27, 30, and 31; Tables 26, 27, 28, 29, 32, 34, and 35) and factory integration (page 156; Tables 47 and 48).]

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Thin-Film Profile Measurement Methods and Reference Materials

NIST is pursuing a multifaceted analytical approach to 2D and 3D compositional profiling. Main objectives of this work are to: (1) develop a quantitative 3D image-depth profiling method with submicrometer lateral resolution using Secondary Ion Mass Spectrometry (SIMS), and to define optimum protocols for ultra-high depth resolution and ultra-shallow profiling by SIMS; (2) develop nondestructive methods for analysis of thickness and composition of multilayered structures using electron microprobe (x-ray) analysis; (3) develop trace analysis methods at nanometer resolution using high-voltage analytical electron microscopy with parallel energy loss spectrometry; and (4) develop profiling reference materials to assist the semiconductor industry.

Image depth profiling by SIMS uses a microbeam ion source to acquire sequential frames and subsequently reconstructs 3D profiles using advanced image processing methods. Proper account is taken of measurement effects such as beam-induced broadening of interfaces and matrix effects on secondary ion yields. This approach is being developed and tested on useful device structures including FIB implant patterns. A second ion-beam development area is ultra-high depth resolution profiling. We are exploring the use of a rotating SIMS sample stage to minimize sputtering-induced roughness as a factor in depth resolution. We recently applied high-depth-resolution profiling to study transient-enhanced diffusion in shallow B^+-implanted Si in collaboration with the University of Florida, and found quite different diffusion behavior in crystalline *vs.* amorphous Si.

Microprobe analysis of multilayer structures is done via a protocol that uses progressive increases in incident electron beam energy and deconvolution of x-ray intensities using a knowledge of the ionization depth distribution function. The analytical electron microscopy work is being applied to the detection and mapping of ion implants in Si and transition metal impurities in SIMOX wafers.

The NIST SRM 2137 has been used in an ISO international round-robin study among 16 laboratories to determine the boron concentration in an unknown epitaxial Si sample by SIMS. The relative standard deviation of the boron determinations in the unknown was 8% among the 16 labs, and only 4% among the 6 U.S. participants. The excellent interlaboratory comparability is directly attributable to the availability of a common certified reference material. NIST also helped to coordinate a round-robin study among 12 U.S. SIMS labs to determine the retained dose of an arsenic-implanted Si sample. In contrast to the boron study, the determinations among labs showed a range of over 60%. These results provide a strong motivation for NIST to develop an Arsenic-Implant Standard Reference Material, which has also been designated a priority item by the SEMATECH Analytical Laboratory Managers Working Group. We have formulated a plan to certify the arsenic dose with an uncertainty of about 1% by neutron activation analysis.

[Thin-film properties and doping distributions are discussed throughout the Materials and Bulk Processes and Interconnect chapters of the NTRS (pages 94, 106, 110, 119, 122, and 128; Figures 17, 25, and 31; Tables 25, 30, 32, 33, and 35. Reference materials are cited as a need on pages 105, 112, and 128; in Figure 31 and in Tables 27 and 35.]

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Radiometric Metrology for Deep Ultraviolet Lithography

The National Technology Roadmap for Semiconductors clearly identifies the path to shorter wavelength photolithography as part of fabrication technology evolution. Improved measurement of absolute dose and uniformity over the exposure field is necessary for DUV lithography. NIST is addressing these issues through improvements to present sources and detectors in the DUV as well as development of new sources, detectors, and more accurate radiometric scales. NIST is also partnering with Lincoln Laboratory in the SEMATECH/DARPA-sponsored 193 nm lithography demonstration project.

An important part of the infrastructure necessary for future work is an ongoing upgrade to the existing Synchrotron UV Radiation Facility (SURF II) which acts as the primary standard for both sources and detectors in the DUV spectral region. This upgrade project (to SURF III) will provide for hardware enhancements to the synchrotron itself, new beamlines dedicated to optical metrology and radiometry, and an increase in storage energy to allow useful emission of radiation down to 2 nm wavelength.

Detailed activities of the DUV metrology program are:

1. Collaborate with Lincoln Laboratory's 193 nm lithography efforts to characterize the properties of UV transmitting materials, e.g., measurements of the index of refraction of quartz and CaF_2.

2. Develop and characterize a new broadband UV source standard based on a high-power microwave discharge with a 0.2% source accuracy goal. Also, develop new improved exposure monitors for intense broadband UV sources used in photoresist stabilization (with a U.S. commercial firm).

3. Develop new DUV wafer-plane dose monitors for measurements at 248 nm and 193 nm (with a U.S. stepper manufacturer).

4. Achieve 0.1% accuracy of UV irradiance from 3 nm to 400 nm (includes SURF II to III upgrade).
   a) obtain absolute beam current measurements on SURF II using a cryogenic radiometer.
   b) develop two new radiometric beamlines on SURF III with instruments.
   c) make source radiance and irradiance comparisons directly with SURF III.

5. Establish traceability of primary standard detectors to SURF III with detector spectral responsivity accuracy goals of 0.2% from 100 nm to 400 nm.

6. Apply polarimetry characterization of optical materials from 3 nm to 400 nm utilizing SURF III.

[Radiometric improvements are behind-the-scenes metrology issues not mentioned in the Lithography chapter of the NTRS. They are clearly necessary for 248 nm (and beyond) for all of the exposure technologies listed in the lower half of Table 16.]

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Electrical Test Structure Metrology

NIST develops electrical test structures to determine metrological, reliability, and process parameters.

Linewidth: Control of critical dimension (CD) is crucial to the manufacturing of advanced VLSI devices. NIST collaborates with Lincoln Laboratory and Sandia with the goal of electrical certification of linewidth calibration standards for 0.18 μm geometries. New single-crystal linewidth test structures with edges defined on crystallographic planes have been produced and are undergoing initial testing. Additionally, since these structures have "ideal" sidewalls, they will be used to quantify systematic offsets encountered between different linewidth measurement techniques, such as electrical, optical, SEM, and SPM, used in semiconductor process characterization. NIST researchers also provide support to industry via development of SEMI standards for critical dimension patterns.

Overlay: Accurate level-to-level overlay is critical for advanced integrated circuits manufacturing. NIST is involved in several collaborative efforts with overlay instrument manufacturers to develop metrology tools for coming generations of VLSI circuits. In one effort, NIST and a tool manufacturer are comparing commercial optical overlay instrument techniques with electrical overlay techniques using a modified voltage-dividing potentiometer test structure developed and patented by NIST. Additionally, a consortium including NIST, SEMATECH, and four overlay tool instrument makers has been initiated to develop and transfer new metrology techniques for locating planar, buried (CMP) features to industry. NIST researchers also provide support to industry via development of SEMI standards for overlay patterns.

Oxide reliability: As gate dielectrics are getting thinner with the aggressive scaling of device geometries, the long-term reliability of these ultra-thin layers is becoming a primary concern. NIST is collaborating with six U.S. semiconductor manufacturers in a joint research effort to understand the physical mechanism of time-dependent dielectric breakdown (TDDB). Pulsed bias measurements have provided evidence that the physical mechanism of dielectric breakdown changes as a function of electric field. These results are being used to develop a physically correct model to describe TDDB for ultra-thin dielectrics. Other work includes investigating highly accelerated wafer-level tests commonly used to characterize oxides in industry and comparing their results with those obtained from long-term stress tests. NIST also is organizing the development of a joint standard between JEDEC (EIA) and ASTM that describes several voltage- and current-ramp test procedures for characterizing ultra-thin dielectrics.

Electromigration: NIST works with standards organizations to develop and evaluate standard test methods and test structures important for reliability evaluations of metal interconnects. Semiconductor manufacturers, Sandia, and universities have been involved in inter-laboratory experiments for measuring metal TCR, joule heating, electrical linewidth, and wafer temperature to establish precision statements and to improve measurement methods for corresponding JEDEC and ASTM standards. Special test structure and experimental test designs have been included in a SEMATECH reliability test-chip program. Significant revisions of two other ASTM standards (for standard test-structure design and for electromigration testing) were completed and submitted for ASTM ballot and industry review. A proposed standard for calculating the model parameters of electromigration was completed and is currently in the JEDEC review process. A JEDEC standard for bond-pad layout has been developed, which is intended to facilitate the conduct of future inter-laboratory experiments involving wafer-level measurements.

[Test structures are called for in general terms on page 94 of the NTRS. The need for standardized test structures is stated on page 104 as a priority need. Quality and reliability concerns related to metal films and dielectrics are discussed on pages 105 and 106 and listed in Table 19. A related discussion on CD and overlay is covered on page 106 and in Table 25.]

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Metrology for Devices and Packages

NIST has made technical and leadership contributions to all of the significant microelectronic device and package thermal standards now in use in the U.S. The most pressing thermal characterization and analysis issues for packages today concern measurement and specification of the thermal environment around the package and the development and characterization of compact thermal model representations for packages. The NIST Package and Device Metrology Project is addressing both of these areas.

Compact Package Thermal Models: The task in this area is to develop methods for validating compact models for system level thermal analysis. A compact model may be thought of as a model that is detailed enough to produce a result with acceptable accuracy but reduced or compact enough to be computationally practical. As the domain being simulated increases in complexity (chip-package-board-system), the details of the component models must be compacted. Currently, work is underway to develop **measurement procedures for extracting the model parameters** for package thermal models similar to the models being developed by the European DELPHI project and for **validating models** using test methods similar to those developed by the EIA JEDEC Committees. Initially, validation procedures will be developed for a quad flat pack on a circuit board in a natural convection environment. Results of this work should be available and published in the early 1997. A second phase of this task is using a validated compact model to simulate the performance of a laptop-like enclosure with an array of heated thermal test chips on a circuit card. This work will be completed by late 1997. This latter work includes CFD simulations, temperature measurements, and experimental flow visualization of the convective patterns.

Thermal Environment: The definition and measurement of convective heat transfer coefficients, h, for package surfaces is a serious problem in the thermal characterization of microelectronic systems. The values for h set the package boundary conditions for simulations. NIST is working on a novel micromachined structure, consisting of a heater and thermocouples on an isolated membrane, for measuring the local heat-transfer coefficient on packages. Initial measurements have been made for a natural convective environment and forced-air measurements are in progress. Simulations have been done for both natural and forced convection. The preliminary results of this work will be reported in late 1996.

[Metrology and modeling of packages are both discussed on page 132 of the NTRS. NIST has long been a strong contributor on these topics. The wide divergence between power levels for hand-held vs. high-performance applications (Table 37) underscores the need for improved package designs (discussion, page 136). These can only be obtained with the aid of improved 3D models and the necessary data on materials properties to support them.]

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Wafer and Chuck Flatness/Thickness

Limited lithographic depth-of-focus budgets for finer features on larger silicon wafers pose new challenges for flatness metrology. Mechanical distortions of wafers induced by conventional vacuum chucks are part of a manufacturing problem that NIST is also addressing. Work on surface preparation of other electronic materials is yet another part of this program.

NIST has developed flat calibration capabilities using a commercial Fizeau interferometer (Wyko Model 6000) to uncertainties approaching 6 nm over wafer diameters of 150 mm. The entire wafer is imaged at once, unlike techniques using scanned probes. That image provides a useful qualitative picture of the flatness, while the quantitative description is extracted from on-line analysis of the image data.

This method is being extended to 300 mm wafers using the same interferometer by applying a technique well known to the optics industry (the Ritchey-Common test). The optical system is in place to allow measurement of as-chucked wafer flatness for 300 mm wafers and, by 4th Quarter 1996, this system will offer traceable flat metrology for 300 mm wafers. The uncertainty will be further reduced with a next-generation interferometer currently under development.

In a parallel development, the NIST team has developed a new concept for measurement of thickness, free-standing bow, and thickness variations. Wafers will be measured at three positions in a transmission infrared interferometer. The wafer is flipped front to back between two of the observations allowing bow to be separated from average thickness and mapped independently. Demonstration of principle is completed and an instrument capable of routine measurements is expected to be completed by 1st Quarter 1997.

NIST capability in flatness measurement will be used to evaluate issues associated with specific vacuum chuck systems as well as to explore new chucking concepts. One important short-term issue is the differing distortions caused by chucks on actual lithography equipment versus those on commercial instruments designed to measure wafer flatness. NIST is developing chucks made of hard, porous ceramics which can be made extremely flat and provide superior support of the wafer from a large number of distributed points.

A novel lap concept has been developed (patent applied for) and applied to both diamond lapping and chem-mechanical polishing (CMP) processes. Rapid, low damage lapping of crystalline substrates (silicon, sapphire) has been demonstrated; potential to reduce wafer fabrication times through combinations of diamond lapping and current processes will be evaluated by 4th Quarter 1996. The new lap concept also has potential to enable rapid pad changing in CMP processes.

[Wafer metrology is described on page 112 of the NTRS. Site flatness (in 2004) on 300 mm wafers is specified to be better than 80 nm over a large field on page 113; Table 26. Flatness figures for planarization are given in Table 22. Flatness metrology is a high-priority topic on page 115; Table 27. Vacuum-chuck flatness is not mentioned in the NTRS but is a serious concern as revealed by direct industry contact. Planarization processes (CMP) that implicitly need flatness measurements are in Figure 18 and discussed on page 99.]

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Optical Scattering for Wafer Surface Metrology

Optical scattering metrology tools are indispensable in modern fab lines mostly for defect and particle sizing and counting. Commercial instruments are almost all laser-based scanning systems that collect scattered light and process the resulting data in different ways. Each of these instruments uses a different subset of the more fundamental bidirectional reflectance distribution function (BRDF). If one considers a small, collimated beam of light impinging on a wafer surface at an arbitrary angle, the BRDF describes the angular-resolved scattering of light into the hemisphere above the wafer. Appropriate integration of the BRDF therefore defines the response of any instrument to a given set of scattering features. Polarization of both the incident and scattered beams has not yet been extensively explored but likely contains additional information that will add to the value of this technique in probing the near-surface volume of materials.

Extensive BRDF measurement capability exists at NIST with wide dynamic range, high angular accuracy, very low instrumentation scatter contributions, and multiple incident wavelengths (visible and UV). This instrument will be especially useful in transferring calibration to commercial tools that employ varied measurement conditions. Work is underway to expand the capability to resolve the polarization states of the incident and scattered light.

The ultimate objective of this work is to develop algorithms that will accurately interpret scatter data. Such capability will then allow NIST to develop standard artifacts and methodologies to extract information about particles, microroughness, contamination, films, and subsurface defects.

Near-term work is aimed at correlating BRDF from bare silicon wafers displaying varying amounts of haze with data taken by commercial haze meters. Once a reliable correlation has been established, a calibration scheme will be developed for a new NIST Standard Reference Material for haze. In addition, wafers deliberately contaminated with real-life particles will be characterized with BRDF metrology to develop an empirical model of scattering from contaminated, microrough surfaces.

Investigations are being initiated to characterize the distribution of 193 nm light scattered from the surfaces and bulk material of fused silica lenses used in a prototype photolithographic exposure tool at MIT Lincoln Lab. Causes of scatter in the exposure tool must be identified and eradicated in order to improve image quality and product yield.

[Optical scattering methods used for detecting particles, haze and microroughness on wafers are not well-quantified today. Needs for measurements are outlined in the NTRS on pages 111, 112, 115, and 119 and also in Tables 26, 27, 28 and 29. The work discussed here complements the spatially-integrated work of Joseph Fine with the SSM (see next page).]

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Non-Destructive Microroughness Characterization of Buried Silicon Interfaces

Fabrication of defect-free ultra-thin (UT) insulating layers (2nm to 5 nm) on silicon requires the development of deposition techniques that do not alter the topography of the silicon substrate. The development of such techniques for making oxide and oxy-nitride UT layers would benefit greatly from having a direct non-contact, non-destructive method for monitoring the buried Si/insulator interface roughness both during and after film growth.

The NIST-invented optical scatter instrument, the scanning scattering microscope (SSM), has been further developed so that interface microroughness of UT insulating layers on silicon can be measured directly -- without destroying the outer, thin insulating layer. This optical-scatter technique generates two-dimensional images of surface defects and microroughness presently with a lateral resolution of about 5 μm. The microroughness sensitivity of the SSM has been substantially improved and is realistically in the sub-angstrom region. Use of calibrated AFM techniques has allowed us to determine the contribution of the outer SiO_2/air interface to the total optical-scatter roughness, and by modeling the two-interface scattering problem, the roughness contribution of the buried Si/SiO_2 interface can be determined.

We are presently measuring the buried interface roughness of UT SiO_2 layers on Si. By combining the use of our SSM with AFM measurements on both pre- and post-stripped SiO_2 layers, we have been able to demonstrate that virtually all of the scattered light intensity is produced at the buried interface. This strongly suggests that the SSM can be used directly (without stripping) to characterize buried-interface topography with very little correction required (probably less than 10%) to account for the roughness of the outer SiO_2 surface.

In the course of these SSM measurements, we have been able to evaluate the roughness sensitivity of our instrument. In its present configuration we can determine differences in rms surface roughness of 0.02 nm (0.2Å).

Also, we plan to evaluate various processing techniques for both the preparation of the Si substrate and for oxide growth to determine the optimum approach for producing defect-free UT insulating layers.

[Microroughness values of 0.1 nm (!!) on wafers are specified in Table 26 of the NTRS for 0.18 um products. Control of microroughness is a high-priority item in Table 27 and also Table 29. Defect limits are described throughout the Materials and Bulk Processes chapter but near-surface defects are not specifically mentioned. Defect detection limits (80 nm will be needed by 1998, decreasing to 20 nm by 2010) imply the use of techniques not presently available. Exploratory work is clearly necessary.]

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High-Accuracy Two-Dimensional Measurements

The ability to place features accurately in 2D has multiple impacts in the electronics industry. Manufacture of reticles, large high-resolution displays, and circuit boards involve different aspects of the same metrology problem.

The situation regarding this critical capability is unusual in that state-of-the-art commercial measuring machines (such as the Nikon 5I or Leica LMS 2010) are so accurate that there is no available source of better 2D measurements from which standards can be established. As such, each user today is "traceable" only to their particular measuring machine. NIST clearly recognizes the industry-wide exposure inherent in this situation and is developing innovative practical approaches to establish convergence in the absence of a conventional standard.

The NIST linescale interferometer is known to provide the most accurate 1D measurements available in the world. Preliminary work has been carried out on algorithms which will allow the use of this tool on the 2D problem. Multiple passes of linear artifacts with different orientations on the customer's measurement machine will provide a reasonable accuracy check. We are also working with industry to design a suitable interlaboratory test (round-robin) to assess the current industry capabilities.

In the shorter term, NIST is working toward a 2D (200 mm x 200 mm) measuring machine at its Gaithersburg, MD facility to test algorithm designs and sensor effects. A larger range machine (750 mm x 750 mm) has been brought on line to make measurements on large grid plates used in PC board and flat-panel display fabrication. The uncertainty (k=2) of measurements on this instrument is 0.4 μm over the full range of the machine.

[Two-dimensional measurements are implicitly needed for controlling overlay capabilities of steppers and mask-making tools. Overlay is listed in table 19 of the NTRS as a show-stopper for 0.18 μm technology. While production of 0.18 μm products is not expected until 2001, NTRS also points out that technology must be available five years earlier to allow the normal process of development and prototyping. Table 18 therefore implies a short-term need for overlay metrology with uncertainty of 5 nm (3σ).]

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Improved High-Temperature Thermocouple Thermometry

Use of thermocouples with wires made of metal alloys is ubiquitous throughout the semiconductor industry. Two assumptions are often made, i.e., that the thermocouples are stable with time and also that the thermocouple measures the difference in temperature between the measuring junction and a reference junction independent of the details of the temperature gradient along the thermoelements. Careful examination of commercial thermocouples shows that these assumptions are often incorrect due to phase changes in the alloy materials and to inhomogeneities, compositional or physical, along the length of the wires. For example, in commercial thermocouple types S, R and B, errors as large as 10 °C at 1350 °C are not uncommon.

NIST is developing improved thermocouples consisting of high-purity Pt and Pd wires that will minimize these errors. Such thermocouples are expected to have errors less than 0.1 °C below about 950 °C and less than 0.5 °C at 1350 °C. To fully realize the commercial capabilities of these thermocouples, accurate determination of the emf-temperature reference function over the entire temperature range is required. NIST has obtained most of the data necessary for deriving that reference function. For some of the high-temperature data, NIST has collaborated with the Istituto di Metrologia "G. Colonnetti," the Italian national standards laboratory. This investigation will be completed in 1996. Preliminary results on this work will be reported at TEMPMEKO '96, a conference on thermometry to be held in Torino, Italy, in September 1996, and at the meeting of the Consultative Committee on Thermometry of the International Committee of Weights and Measures, also in September 1996. The final results will be published in an archival journal.

[Temperature control by various means is outlined in Figure 31 on page 129 of the NTRS. The temperature errors in RTP are known to be large. Need for improvement is described on page 122 and in Table 32 and is a high-priority item in Table 33. This work provides the best available thermocouple for high-temperature measurements and forms the foundation for follow-on efforts aimed at improving the situation in the RTP environment.]

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Micromechanical Measurements†

Thin films are an essential component of all advanced electronic devices. Knowledge of their micromechanical material properties and behavior is fundamental to design, manufacturability, and reliability of advanced integrated circuits and interconnect systems. This NIST effort develops measurement, analysis, and modeling techniques for micromechanical properties. We provide accurate material property information and experimentally verify finite element and other theoretical model predictions. The effort concentrates on material configurations of industrial significance. Project thrusts are in mechanical properties of thin films, high-resolution experimental mechanics, and a new effort in stress-voiding studies.

The *mechanical properties of thin films* differ from those of bulk material because the deposition methods are much different than for bulk metals. A method for measuring mechanical properties of thin films has been developed and applied to suspended metal films. The technique and resulting data are intended to promote the use of advanced mechanical engineering methods and improve the mechanical reliability of advanced electronic materials and assemblies. For example, a collaboration with Sandia National Laboratories has demonstrated that sputtered copper metal thin films are much stronger than e-beam evaporated films. We regularly measure fatigue of metal films for several tens of thousands of cycles. In-situ TEM observations during tensile strain to failure of copper films showed that cracks formed easily and propagated both through the grains and along the grain boundaries, but only a few dislocations were seen. In a collaboration with Ford Microelectronics, our apparatus has allowed us to acquire previously unattainable data on 13 μm thick epitaxy silicon for micromachined sensors.

We have developed electron beam moiré as an *experimental mechanics* technique for examining mechanical displacements in very small fields. Its advantage is the capability to write gratings with pitches much smaller than the wavelength of light. Our gratings now have 0.1 μm pitch over a 50 μm field of view. The technique has been successfully applied to examination of thermomechanical displacements in cross-sectioned specimens of plated-through-holes. Recently we evaluated interconnect structures in multichip modules (with USAF Rome Laboratories and General Electric) and ball grid arrays (with Digital Equipment Corporation). This year we have improved the capability of the technique by producing double and quadruple line density grids and, with new additions to the apparatus, we have demonstrated that orthogonal gratings could be written. A program of experiments on conductive adhesives was initiated in collaboration with 3M, Ablestik, and AI Technology. Preliminary measurements are giving promising data.

The study of *stress voiding in thin films,* initially supported by a NIST/NRC postdoctoral award, is our newest research area. This important electrical failure mode, is related to the same microstructural features that control mechanical behavior. Severe triaxial stress states develop in passivated narrow metallizations and are manifested in different forms for different grain orientations. Understanding and solving the problems of void formation is essential to the continued development of metallizations on a submicron scale. We have demonstrated the feasibility of using backscatter Kikuchi diffraction (BKD) to obtain crystallographic data from narrow metallizations which had undergone stress-induced voiding. In a collaboration with Cornell's National Nanofabrication Facility, nearly 300 BKD patterns have been collected and indexed in digitized form. We have begun analyzing these patterns to correlate crystallographic features with void formation. To our knowledge, such data have not been acquired before.

[The NTRS states "... Materials characterization and process model accuracy in both two and three dimensions must improve to predict adequately the performance and reliability of future device structures" and calls for standard tests and measurement procedures for thin film systems as well as "aggressive materials, process, and film characterizations." The Interconnect Working Group calls for "standard test structures and methods for characterizing electromigration, stress voiding, and interfacial-related failure mechanisms in interconnects."]

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Solderability Measurements and Optimization[†]

As the dimensions of electronic devices decrease, interconnection densities increase, and surface-mount replaces through-hole connections, more stringent demands are placed on solder and the soldering process. Good first-pass solderability is an increasingly important industrial goal, especially for surface-mount connections and ball grid arrays. To meet the need for improved solder joint reliability, NIST is developing measurements, test techniques, and scientific guidelines for both Pb-Sn and Pb-free solders that manufacturers can use to evaluate components for solderability before committing them to the production line and applying them in the evaluation of solder joint designs for their manufacturability and reliability. For this purpose, measurements and modeling of wetting balance solderability tests, area-of-spread solderability tests, and solder wetting phenomena are underway.

NIST scientists are evaluating the effects of wetting and solder joint reactions on solderability, manufacturability, and reliability. Reactions between Sn-based liquid solders and Cu produce brittle, poorly-wettable, intermetallic compounds (Cu_3Sn and Cu_6Sn_5) along the solder-Cu interface at typical soldering temperatures. The same intermetallics are produced by solid-state reactions when components are stored at room temperature. NIST measurements have shown how intermetallic formation and oxidation can affect solderability. These results are being used to design improved solderability tests, particularly accelerated tests. A NIST-designed accelerated test using steam-aging techniques to allow more rapid testing is under consideration by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) in collaboration with the IPC Steam Aging Task Group.

Since industry finds that the presently used wetting-balance tests are not sufficiently reliable, improved tests are needed. Predictive models are being developed for the rate and extent of reactive wetting of solder during area-of-spread and wetting balance solderability tests. Complicating factors in these models are solute diffusion and the Marangoni flow from temperature gradients expected under these conditions. These and related efforts being pursued in collaboration with the IPC Wetting Balance Task Group are directed toward developing an improved solderability test to provide more reproducible measurements of initial solderability and the loss that can occur during storage.

[This topic is not explicitly mentioned in the NTRS but is of continuing concern to device makers and their customers. This issue is also driven by the smaller pitch and footprint of leads on surface mount devices and by concerns raised by the advent of lead-free solders (page 138) which will inevitably involve changes in soldering techniques.]

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Hygrothermal Expansion of Polymer Thin Film[†]

Polymers are widely used in electronic packaging for applications such as interlayer dielectrics, underfill in ball grid arrays, die attach adhesives, heat sink adhesives, conductive adhesives, encapsulants and substrates for high density interconnects. In many of these applications, the polymer is in the form of a thin film adhered to materials of radically different physical properties. Knowing and predicting the dimensional stability of materials in semiconductor packaging and interconnects are important for enhancing the performance and reliability of complex materials assemblies. The physical properties of such films, especially in a constrained configuration, can be significantly different from those of the same material in bulk form or in free-standing films. Traditional expansivity measurements based upon mechanical displacement are not sensitive to the small dimensional changes exhibited by the thin films encountered in electronic packaging and interconnects.

This effort has the primary objective of providing industry with robust measurement tools and data for characterizing the dimensional stability of polymers. In particular, the project is focused on the impact of changes in temperature and humidity on the out-of-plane dimensions of thin films. NIST has designed, built and demonstrated a capacitor cell with outstanding sensitivity for measuring the out-of-plane expansion of polymer films. The project has three sets of activities: (1) determining the accuracy and precision of the technique applied to a variety of polymer measurements; (2) working with standards-setting bodies to explore the desirability of introducing the technique as a standard method for measuring thermal and hygroscopic expansion; and, (3) providing industry with materials property data on selected packaging materials.

In the first set of activities related to precision and accuracy, we are conducting extensive studies to determine the measurement uncertainties and limitations of the current capacitance-cell design and measurement method. This work is being conducted with the assistance of the Statistical Engineering Division. In the second set of activities, we plan to work with the test methods committees of IPC, SEMI, and ASTM to have the capacitance technique considered as an additional standard test method for the measurement of thermal expansion for cases in which the existing standards are inappropriate. Thirdly, in the course of the work, data on several materials of importance to the electronics industry will be generated which will be incorporated in the SRC-sponsored database maintained by CINDAS at Purdue. We expect to provide measurement expertise to consortia such as the NCMS-sponsored consortium on PWBs and the ITRI-sponsored October Project which is directed toward making high density interconnects compatible with chip scale packaging and direct chip attach.

[The NTRS pinpoints high-density substrates as an important enabling technology needed to capitalize on developments in chip-scale packaging and high-density interconnection. In addition, polymer dielectrics and standards for materials and processing are mentioned. This project is working to introduce the measurement standards needed to describe thin films used in these applications.]

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Improved Radiation Thermometry for RTP Control using Multispectral Thermal Imaging

The rapid thermal processing (RTP) environment presents unique challenges to accurate measurement of temperature. Common approaches using optical pyrometry are complicated by the unknown emissivity on the wafer backside and the huge 60 Hz, 3-phase ripple signals generated by the heating lamp arrays. Even calibrations using special wafers with embedded thermocouples are further complicated by the fact that modern equipment rotates the wafer in-process to improve temperature uniformity.

In a new effort this year, NIST has proposed and will be examining the viability of a new approach to optical pyrometry for RTP control. The idea is to measure the optical emission of the wafer at considerably longer wavelengths than is conventionally done (5 to 8μm) and to determine absolute temperature by curve-fitting a series of intensities measured at these longer wavelengths. Examination of the basic radiation physics indicates that such a technique will offer considerably less dependence of measured temperature on wafer emissivity. Since these wavelengths are well beyond the cutoff of quartz, stray light from the heating lamps is also expected to be much less of a problem.

A parallel effort also addresses making better calibration wafers using thin-film thermocouples and/or a new Pt/Pd elemental thermocouple with enhanced stability in strong thermal gradients.

Work to be completed in 4th Quarter 1997 will focus on verifying the operation of a single-point multispectral pyrometer on a commercial RTP testbed. Assuming successful results, work on an imaging array will begin in 1998.

Dr. Dave DeWitt, a well-known authority in this field, has joined this effort at NIST on sabbatical from Purdue University.

[Strong support for this effort appears on pp. 122 of the NTRS where it states, "RTP offers the potential to significantly reduce thermal budget, while affording single-wafer granularity and cluster compatibility.... Improving of RTP temperature control ability ... will be the key." This is underscored in Table 33 on pp. 124]

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High-Frequency Characterization of Interlevel Dielectrics for Integrated Circuits

Improved performance from both dielectrics and conductors will be a pivotal part of realizing the advantages of feature size scaling for interconnect-dominated chip designs. Lowering the dielectric constant (k) of the intermetal dielectric is a favored approach. Many of the candidate materials for this application are "foreign" in the sense that they have not been widely used in IC fabrication before and are difficult to integrate into the process sequence.

The focus of this effort is to provide the metrology necessary to make sure that the performance of these new materials in propagating high-speed pulses on-chip lives up to the promise that improvements in the low-frequency dielectric constant would indicate. This is accomplished by making frequency-domain measurements on a series of simple transmission line structures fabricated with the materials in question and rigorously extracting both the real and imaginary parts of the complex dielectric constant as a function of frequency to 20 GHz.

This work is an extension of earlier methods used to characterize circuit board materials and takes advantage of existing software tools.

The effort in Calendar Year 1996 has focused on developing the test structure layouts and metrology capability at NIST in Boulder, CO. It has proven to be more difficult than expected to obtain the transmission line test structures fabricated with candidate low-k materials. NIST is currently collaborating with several major domestic device suppliers and SEMATECH to realize test wafers that can be fabricated with existing facilities and still yield accurate results. It is, however, expected that initial results of the measurement for conventional (oxide) intermetal dielectrics made by a foundry will be available by 4th Quarter 1996.

[The use of low-k dielectric appears several times in the Potential Solutions roadmaps on pages 100-102. In the Priority of Technology Needs section (for interconnect) on page 103, it states, "It is expected that low dielectric-constant materials will have an even greater impact than low-resistance metals (on performance)".]

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Thin-Film Reference Materials

All of the layers which combine to make a modern IC can be generally characterized as thin films. Some of these layers, e.g., grown gate oxide, have limited structural possibilities and have evolved with multiple methods of characterization which can be cross-checked (in our example, ellipsometry and specific capacitance). Other critical layers, notably those used in the interconnect sequences, are deposited during processing, have a broad range of structural possibilities and are not amenable to in-situ metrology. In the latter case, having a well-characterized reference material for comparison which represents the proper structure and/or composition is invaluable as an analytical reference in manufacturing.

A prioritized list of needs for thin-film reference materials was developed in collaboration with the SEMATECH Analytical Lab Manager's Working Group (ALMWG). Thin films of titanium nitride (100 nm thick), often used as diffusion barriers for interconnect, emerged as the top priority for development of a reference material.

NIST has set up facilities to deposit TiN films on silicon and is using a combination of X-ray methods to characterize them. X-ray reflection is used to fundamentally obtain the thickness of these films and thereby to calibrate fluorescence equipment which is often used commercially for the same purpose. Samples of the TiN reference material will be available on request in 3rd Quarter 1996. If these samples are found to adequately fill the need, NIST will move on to address the next item on the ALMWG list which is boron-and-phosphorus doped CVD oxides.

(It is important to note that these reference materials are not subject to same intense analysis and certification requirements as NIST Standard Reference Materials. Rather, it is intended that these be useful materials that are placed in user's hands in a timely fashion to address a series of short-term technology issues.)

[The impetus for NIST to develop these materials comes from a letter by Jim Owens, SEMATECH COO, to Mr. Robert Scace at NIST dated September 13, 1995. Item 5 in the letter's attached table, "Metrology Capabilities for IC Manufacturing," specifically calls for TiN barrier layers. The details of this work were established by consensus vote within the SEMATECH ALMWG on 3/5/96.]

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High-Resolution X-Ray Spectrometer for Chemical Analysis

The familiar energy dispersive x-ray spectrometer is an ubiquitous accessory to the scanning electron microscope (SEM). It provides fast, convenient elemental analysis of whatever the SEM is imaging. The conventional lithium-drifted silicon or germanium X-ray detectors used for these spectrometers limit the energy resolution to the order of 100 eV and tend to give noisy responses to the low energy X-rays emitted by important light elements used in device fabrication, e.g., boron, carbon, nitrogen, and oxygen.

NIST has used a microcalorimetry technique to create an entirely new X-ray detector with energy resolution about an order of magnitude better than can be achieved with conventional detectors. In fact, the resolution of the NIST microcalorimeter in energy dispersive mode rivals that of complex wavelength dispersive electron microprobes. Output of the NIST detector is compatible with the same multichannel analyzers used in conventional spectrometers. The improved resolution of the NIST microcalorimeter allows strongly overlapping x-ray peaks to be separated, e.g., the nitrogen K-line and the titanium L-lines in TiN. Improved resolution also suppresses the X-ray background at low energies, significantly enhancing the detectability of light elements.

The NIST instrument uses cryogenic techniques, and an important part of the development has been to build a refrigeration system that is small and robust for industrial use. The resulting detector is somewhat larger than conventional ones but has been successfully mated to the standard port of a commercial SEM.

Work in Calendar Year 1996 is directed at hardening the instrument and improving the effective area of the detector to enhance the counting rate. Calendar Year 1997 efforts will be directed at constructing a beta tool to be installed on a commercial SEM at NIST in Gaithersburg, MD for use by industrial visitors.

[Detailed guidance regarding instrumentation is outside the scope of the NTRS. However, strong industrial support for this effort has been registered by the SEMATECH Analytical Lab Managers Working Group.]

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